Course Code: ELE-522
Course Title: EDA Tools
Number of Credits: 04 **Total Hours: 60** **Total Marks: 100**
Effective from AY: 2022-23

Prerequisites for the course

Should have studied Digital Communication Systems

Objectives of Course

This course is intended to:

- Familiarize the students with industry oriented EDA tools.
- Teach Quartus, ISE compilations and programming and its use for design and analysis.
- Enable the student to extract various design parameters from simulation results.

Course Content (minimum 10 to be studied/implemented)

Study of JTAG, Modelsim Syntax study.
1. Study of Phases of Quartus compilations.
2. Study of phases of ISE compilations
3. Testing logic using ChipScope-I.
4. Testing logic using ChipScope-II
5. Parallel implementation of CRC.
6. Serial implementation of CRC.
7. FIFO implementation
8. Pulse stretcher
9. Test bench using Modelsim-I
10. Test bench using Modelsim-I
11. Test bench using Modelsim-I
12. Test bench using Modelsim-I

Pedagogy

Lectures/FLIPPED CLASSROOM/Experiential Learning

Course Outcome

The students will,

- Perform compilation using Quartus and ISE software.
- Analyse logic using Chipscope-I and II.
- Develop the Test benches using Modelsim-I

References/Readings

1. Design through Verilog HDL By T. R> Padmanabhan & Sundari. IEEE press, Wiley Interscience.
2. http://www.xilinx.com/itp/xilinx7/help/iseguide/html/ise_fpga_design_flow_overview.htm
3. Hands on experience on altera development board by J.S.Parab,etal: Springer Netherland 2018(ISBN 978-81-322-3769-3)

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