Course Code: ELE-506
Course Title: Digital System Design
Number of Credits: 04 **Total Hours: 60** **Total Marks: 100**
Effective from AY: 2022-23

Prerequisites for the course		
Should have studied digital electronics at the graduate level		
Objectives of Course		
This course is intended to, • Teach principles of combination and sequential logic design • Develop implementation skills using hardware description languages. • Teach and familiarize with industry technologies such as Memory, CPLDS, FPGA.		
Course Content		
Unit I	**Introduction**	**6 Hours**
About Digital Design, Analog versus Digital, Electronic Aspects of Digital Design, PLD's, ASIC, Digital Design level. Digital Concept and Number System: General Positional number system conversions, Operation, BCD, Gray Code,Character Codes, Codes for Actions, Conditions, and States nCubes and Distance, Codes for Detecting and Correcting Errors, Error-Detecting Codes, Error-Correcting and Multiple Error-Detecting Codes, Hamming Codes, CRC Codes, Two Dimensional Codes, Checksum Codes, m-out-of-n Codes, Codes for Serial Data Transmission and Storage, Parallel and Serial Data, Serial Line Codes		
Unit II	**Combinational Logic Design Principles**	**4 Hours**
Switching Algebra, Combinational-Circuit Analysis, Combinational-Circuit Synthesis, and Timing Hazards.		
Unit III	**Hardware Description Languages**	**4 Hours**
HDL-Based Digital Design, The VHDL Hardware Description Language, The Verilog Hardware Description Language		
Unit IV	**Combinational Logic Design Practices**	**4 Hours**
Documentation Standards, Circuit Timing, Combinational PLDs, Decoders, Encoders, Three-State Devices , Multiplexers, Exclusive-OR Gates and Parity Circuits , Comparators, Adders, Subtractors, and ALUs , Combinational Multipliers, Exclusive-OR Gates and Parity Circuits , Comparators, Adders, Subtractors, and ALUs , Combinational Multipliers.		
Unit V	**Sequential Logic Design Principles & Practices**	**12 Hours**

Bistable Elements, Latches and Flip-Flops, Clocked Synchronous State-Machine Analysis, Clocked Synchronous State-Machine Design, Designing State Machines Using State Diagrams, State-Machine Synthesis Using Transition Lists, Another State-Machine Design Example, Decomposing State Machines, Feedback Sequential-Circuit Analysis, Feedback Sequential-Circuit Design, Features ,Sequential-Circuit Design with VHDL , Sequential- Circuit Design with Verilog, Sequential-Circuit Documentation Standards , Latches and Flip-Flops ,Sequential PLDs , Counters, Shift Registers, Iterative versus Sequential Circuits , Synchronous Design Methodology , Impediments to Synchronous Design , Synchronizer Failure and Metastability		
Unit VI	**Memory, CPLDS**	**10 Hours**
Read-Only Memory, Read/Write Memory, Static RAM, Dynamic RAM, Complex Programmable Logic Device		
Unit VII	**Field Programmale Gate Array**	**10 Hours**
Introduction, FPGA Architectures, Configuration: SRAM-Based FPGAs and Antifuse Permanently Programmed FPGAs, Chip I/O, Circuit Design of FPGA Fabrics, Architecture of FPGA Fabrics, FPGA Soft-core Processor Development flow.		
VIII	**Neural Networks on FPGA**	**10 Hours**
Introduction, Designing a Neuron, Activation functions, Design of layers, Training and validations, Hardware verification, Case study using PYNQ/VITIS AI framework.		
Pedagogy		
lectures/ Experiential Learning		
Course Outcome		
The student will, ● Understand principles of combination and sequential logic design ● Leverage Hardware description languages for realization of combinational and sequential designs ● Understand the architecture of field programmable gate array.		
References/Readings		

1. Digital Design Principles and Practices, by John F. Wakerly, Prentice Hall's Fourth Edition.
2. Digital System Design using VHDL: Charles. H.Roth ; PWS (1998)
3. Scott Hauck and Andre DeHon , Reconfigurable Computing, Morgan Kaufmann, 2008
4. Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer, “Logic Synthesis,” McGraw-Hill, USA, 1994.
5. Neil Weste and K. Eshragian,”Principles of CMOS VLSI Design: A System Perspective,2nd edition, Pearson Education, 2000.
6. Kevin Skahill, “VHDL for Programmable Logic,” Pearson Education, 2000. M.N.O. Sadiku, Elements of Electromagnetics 2nd Edition) , Oxford University press, 1995.